## REMARKS

Claims 98 - 135 are now pending in this case. Claims 1 - 97 have been canceled without prejudice. Claims 98, 101-102, 106-108, 110, 119-120, 124, and 126 have been amended. New claims 127-135 have been added. Applicants reserve the right to pursue the original claims and other claims in this and other applications. Applicants respectfully request reconsideration of the subject application in light of the above claim amendments and the following remarks.

Claims 98-101 and 107-123 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nozaki et al. (US 6,570,222). This rejection is respectfully traversed.

Independent claims 98, 107, and 119 each recite, *inter alia*, a method of forming an image sensor comprising "forming an isolation gate," which is used to inhibit electron flow. The above claim feature is not disclosed by Nozaki.

Nozaki discloses using an element isolation region having an STI structure in place of the LOCOS. Nozaki does not disclose any additional structure, much less an isolation gate, to isolate adjacent pixels. Element 13b in Nozaki is a gate electrode of a reset or address transistor (see, col. 10, ll. 41-43) and plays an active part in the operation of the pixel. In the Background Of The Invention section, Nozaki discloses that the gate electrode 13b is electrically connected to the drain region 14a and amplifies electrical signals. Nozaki does not disclose that its reset or address gate electrode 13b is an isolation gate as recited in claims 98, 107, and 119, which prevents charge from moving from one pixel to another. Independent claims 98, 107, and 119 thus patentably distinguish over Nozaki and are allowable.

Moreover, independent claim 98 recites that "said isolation gate extends beyond said isolation region and over at least a portion of a connection region formed adjacent to said isolation region." Nozaki does not teach or suggest this claim feature. As figure 7 of Nozaki shows, the entire reset/address transistor 13b is formed over the STI and does not extend beyond the STI. Therefore, Nozaki does not disclose the

above feature in claim 98. Independent claim 98 thus patentably distinguishes over Nozaki and is allowable for the above additional reason.

To advance the allowance of the subject application, independent claim 107 has been amended to recite "forming an isolation gate ... substantially surrounding said photosensor." Nozaki does not teach or suggest this claim feature. Figures 8-15 of Nozaki show top views of the photodiode and the reset or address gate electrode 13b where the gate electrode 13b is formed side-by-side with the photodiode and does not surround the photodiode. Therefore, independent claim 107 patentably distinguishes over Nozaki and is allowable for the above additional reason.

Similarly, independent claim 119 has been amended to recite "forming an isolation region substantially surrounding said pixel." As applicants submitted above, Nozaki does not teach or suggest this claim feature. Therefore, independent claim 119 is allowable for the above additional reason.

Claims 99-101, 108-118, and 120-123 depend from independent claim 98, 107, or 119 and are therefore patentable at least for the reasons mentioned above. In view of the above, the subject rejection has been overcome; withdrawal of the same is respectfully requested.

Claims 102-106 and 124-126 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Nozaki et al. in view of Casper (US 5,835,433). This rejection is respectfully traversed.

Applicants respectfully disagree that Nozaki suggests that it be combined with Casper to arrive at the claimed invention. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. MPEP § 2143.01.

In fact, Nozaki provides contradictory teachings as to the power supply voltage. In one part of the cited portions, Nozaki discloses that current CMOS image

sensors employ a power supply voltage of 3.3V or higher but expects that CMOS image sensors with a lower power supply voltage will be developed to decrease the size and power consumption of the imaging device (see, col. 2, ll. 44-49). In the other part of the cited portions, Nozaki discloses that a reduced power supply voltage at the readout gate electrode 13a can increase image lags and noise and lower sensitivity of the device (see, col. 2, ll. 28-36). When taken the above disclosures as a whole, Nozaki does not suggest that a voltage be applied to an isolation gate, which does not even exist in Nozaki as applicants submitted above.

Moreover, there is no motivation evident in either Nozaki or Casper that their teachings should be combined. Therefore, independent claims 102 and 124 are not obvious over the cited references.

Claims 103-106 and 125-126 depend from independent claim 102 or 124 and are patentable at least for the reasons mentioned above. In view of the above, the subject rejection has been overcome; withdrawal of the same is respectfully requested.

In view of the foregoing, each of the presently pending claims in this application is believed to be in condition for allowance. Accordingly, the Examiner is respectfully requested to review and pass this application to issue.

Respectfully submitted,

Dated: April 17, 2006

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